Claim Amendments

1. (currently amended) A method ~~for enhancing performance of an electronic device having a host module operatively connected to a memory device via a bus system, the bus system comprising a plurality of signal lines and N data lines for conveying signals and data between the host module and the memory device, wherein the host module is operable in a plurality of data modes, said plurality of data modes including at least one data mode that uses M data lines to convey data between the host module and the memory device, with M smaller than N, leaving (N-M) unused data lines in the bus system~~, ~~said method~~ comprising:

providing in [[the]] a memory device a module for generating at least one further signal, the memory device operatively connected to a host module via a bus system comprising one or more signal lines and N data lines for conveying signals and data between the host module and the memory device, wherein the host module is operable in a plurality of data modes, said plurality of data modes including at least one data mode that is designated to use M data lines to convey data between the host module and the memory device with M smaller than N, leaving (N-M) unused data lines in the bus system; and

causing an exchange of data, based on said at least one further signal, between the host module and the memory device using at least one of the unused data lines even when the host module is operated in said at least one data mode.

2. (original) The method of claim 1, wherein said at least one further signal comprises a command signal, conveyed to the host module on another one of the unused data lines.

3. (currently amended) The method of claim 2, wherein said at least one further signal further comprises a clock signal conveyed to the host module on yet another one of the unused ~~used~~ data lines.

4. (original) The method of claim 1, wherein N is equal to 8 and M is equal to 4, leaving 4 unused data lines, and wherein said at least one further signal comprises a clock signal conveyed from the memory device to the host module on another one of the unused data lines, and a

command signal conveyed between the host module and the memory device on yet another one of the unused data lines.

5. (original) The method of claim 4, wherein said at least one of the unused data lines comprises two unused data lines for carrying out the exchange of data in a differential manner.

6. (currently amended) The method of claim 1, wherein the host module is disposed in an electronic device and the electronic device is operable in a serial peripheral interface ~~(SPI)~~ mode and the bus system further comprises a further signal line for conveying a chip select ~~(CS)~~ signal from the host module to the memory device, and wherein the further signal is conveyed from the memory device to the host module on the further signal line.

7. (original) The method of claim 6, wherein the further signal comprises a command signal.

8. (original) The method of claim 6, wherein N is equal to 8 and M is equal to 4, leaving 4 unused data lines for carrying out the exchange of data.

9. (original) The method of claim 8, wherein exchange of data is carried out in two differential pairs.

10. (original) The method of claim 1, wherein N is equal to 8 and M is equal to 1, leaving 7 unused data lines, and wherein said at least one further signal comprises a clock signal conveyed from the memory device to the host module on another one of the unused data lines, and a command signal conveyed between the host module and the memory device on yet another one of the unused data lines.

11. (original) The method of claim 10, wherein said exchange of data is carried out on a different one of the unused data lines.

12. (original) The method of claim 11, wherein said exchange of data is carried out on two or more different unused data lines.

13. (currently amended) An electronic device ~~for use in conjunction with a memory device~~, comprising:

a host module; and

a bus system operatively connecting the host module to [[the]] a memory device, the bus system comprising ~~a plurality of~~ one or more signal lines and N data lines for conveying signals and data between the host module and the memory device, wherein the host module is operable in a plurality of data modes, said plurality of data modes including at least one data mode ~~that uses~~ designated to use M data lines to convey data between the host module and the memory device, with M smaller than N, leaving (N-M) unused data lines in the bus system, and wherein the memory device is capable of generating at least one further signal, for causing an exchange of data, based on the further signal, between the host module and the memory device using at least one of the unused data lines even when the host module is operated in said at least one data mode.

14. (original) The electronic device of claim 13, wherein the memory device comprises an embedded module for generating said at least one further signal.

15. (original) The electronic device of claim 14, wherein said at least one further signal comprises a command signal conveyed to the host module on another one of the unused data lines.

16. (original) The electronic device of claim 15, wherein said at least one further signal further comprises a clock signal conveyed to the host module on yet another one of the unused data lines.

17. (original) The electronic device of claim 13, comprising a mobile phone.

18. (currently amended) The electronic device of claim 13, comprising a [[PDA]] personal data assistant device.

19. (currently amended) The electronic device of claim 13, operable in a serial peripheral interface, wherein the bus system further comprises a further signal line for conveying a chip select ~~(CS)~~ signal from the host module to the memory device, and wherein the further signal is conveyed from the memory device to the host module on the further signal line.

20. (original) The electronic device of claim 19, wherein the further signal comprises a command signal.

21. (original) The electronic device of claim 13, comprising a software program, responsive to said at least one further signal, for processing the data exchanged between the host module and the memory device on at least one of the unused data lines.

22. (currently amended) A memory device ~~for use in conjunction with a host module via a bus system, the bus system comprising a plurality of signal lines and N data lines for conveying signals and data between the host module and the memory device, wherein the host module is operable in a plurality of data modes, said plurality of data modes including at least one data mode that uses M data lines to convey data between the host module and the memory device, with M smaller than N, leaving (N-M) unused data lines in the bus system, said memory module~~ comprising:

a module for generating at least one further signal configured to be conveyed to a host module via a bus system, the bus system comprising one or more signal lines and N data lines for conveying signals and data between the host module and the memory device, wherein the host module is operable in a plurality of data modes, said plurality of data modes including at least one data mode that uses M data lines to convey data between the host module and the memory device, with M smaller than N, leaving (N-M) unused data lines in the bus system; and

a sub-bus system operatively connecting the module and at least some of the unused data lines for causing an exchange of data, based on the further signal, ~~between the host module and the memory device~~ using said at least some of the unused data lines even when the host module is operated in said at least one data mode.

23. (original) The memory device of claim 22, wherein said at least one further signal comprises a clock signal conveyed to the host module one another one of the unused data lines.

24. (original) The memory device of claim 23, wherein said at least one further signal comprises a command signal conveyed to the host module on yet another one of the unused data line.

25. (original) The memory device of claim 22, wherein the module for generating said at least one further signal comprises a micro-controller.

26. (original) The memory device of claim 22, wherein the module for generating said at least one further signal comprises an input/output device.

27. (original) A software program product embodied in a memory device, the memory device for use in conjunction with a host module via a bus system, the bus system comprising a plurality of signal lines and N data lines for conveying signals and data between the host module and the memory device, wherein the host module is operable in a plurality of data modes, said plurality of data modes including at least one data mode that uses M data lines to convey data between the host module and the memory device, with M smaller than N, leaving (N-M) unused data lines in the bus system, said software program comprising:

a code for generating at least one further signal; and

a code for causing an exchange of data, based on the further signal, between the host module and the memory device using said at least some of the unused data lines even when the host module is operated in said at least one data mode.

28. (original) The software program product of claim 27, wherein said at least one further signal comprises a command signal.

29. (original) The software program product of claim 27, wherein said at least one further signal comprises a clock signal.

30. (original) A software program product embodied in an electronic device for use in conjunction with a memory device, wherein the electronic device comprises

a host module;

a bus system operatively connecting the host module and the memory device, the bus system comprising a plurality of signal lines and N data lines for conveying signals and data between the host module and the memory device, wherein the host module is operable in a plurality of data modes, said plurality of data modes including at least one data mode that uses M data lines to convey data between the host module and the memory device, with M smaller than N, leaving (N-M) unused data lines in the bus system, and wherein the memory device is adapted to generate at least one further signal to cause an exchange of data, based on the further signal, between the host module and the memory device, said software program comprising:

a first code for receiving the further signal; and

a second code, responsive to the further signal, for causing the host module to facilitate said exchange of data using at least some of the unused data lines even when the host module is operated in said at least one data mode.

31. (currently amended) The software program of claim 30, wherein the electronic device is operable in a serial peripheral interface ~~(SPI)~~ mode, and the bus system further comprises a further signal line for conveying a chip select ~~(CS)~~ signal from the host module to the memory device, and wherein the first code recognizes the further signal when the further signal is conveyed from the memory device to the host module on the further signal line.

32. (new) An electronic module comprising:

a processor configured to communicate with a memory device via a bus system, the bus system comprising one or more signal lines and N data lines for conveying signals and data between the host module and the memory device, wherein the host module is operable in a plurality of data modes, said plurality of data modes including at least one data mode designated to use M data lines to convey data between the host module and the memory device, with M smaller than N, leaving (N-M) unused data lines in the bus system, and wherein the memory device is capable of generating at least one further signal, for causing an exchange of data, based

on the further signal, between the host module and the memory device using at least one of the unused data lines even when the host module is operated in said at least one data mode.

33. (new) The electronic module of claim 32, wherein said at least one further signal comprises a command signal, conveyed to the host module on another one of the unused data lines.

34. (new) A memory module, comprising:

means, operatively connecting the module and at least some of the unused data lines, for causing an exchange of data with a host module via a bus system, the bus system comprising one or more signal lines and N data lines for conveying signals and data between the host module and the memory device, wherein the host module is operable in a plurality of data modes, said plurality of data modes including at least one data mode that uses M data lines to convey data between the host module and the memory device, with M smaller than N, leaving (N-M) unused data lines in the bus system; and

means for generating at least one further signal, so that said exchange of data is based on the further signal, using said at least some of the unused data lines even when the host module is operated in said at least one data mode.

35. (new) The memory module of claim 34, wherein said generating means comprises an input/output means.